Assignment 4

Sam Scevenels

The interrupt sequence took 6.3us in my implementation.

This corresponds with 252 clock cycles or 84 cycles where the risc is enabled.

This value is dependent on the length of the interrupt handler however.

So a more accurate value is 65 + irq\_handler() (irq\_handler was 19 cycles)

I also made the timer counter clear the interrupt reset flag after it cleared the interrupt, so that clearing the interrupt only requires 1 command.

Screenshots:

Full interrupt duration  
A screenshot of a computer

AI-generated content may be incorrect.

IRQ\_handler duration

A screen shot of a computer

AI-generated content may be incorrect.